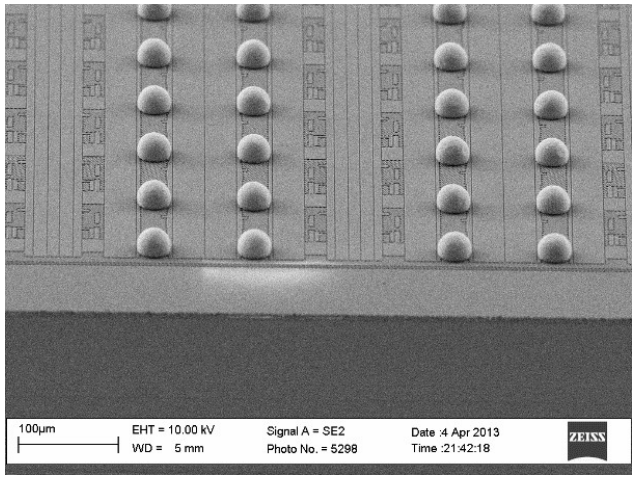
Development of advanced silicon pixel detectors at HIP and RBI for CMS Phase II Upgrade

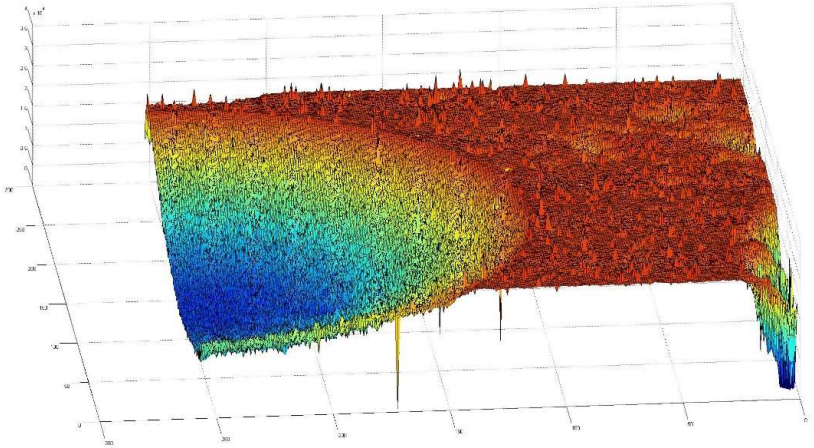
J.Härkönen [1)], J. Ott [2)], A. Gädda [2,3)], A. Karadzhinova-Ferrer [1)], M. Kalliokoski [1)], S. Kirschemann [2)],, V. Litichevskyi [2,4)], E. Brücken [2)] and P. Luukka [2)]

[1)] Ruđer Bošković Institute, Bijenička cesta 54, 10000 Zagreb, Croatia
[2)] P.O.Box 64 (Gustaf Hällströmin katu 2), FI-00014 University of Helsinki, Finland
[3)] Advacam Oy, Tietotie 3, FI-02150 Espoo, Finland
[4)] Specom Oy, Tekniikantie 2 A 326, 02150 Espoo, Finland

contact: name + @helsinki.fi or @irb.hr

http://lnr.irb.hr/PaRaDeSEC/
http://research.hip.fi/hwp/cmsupg/

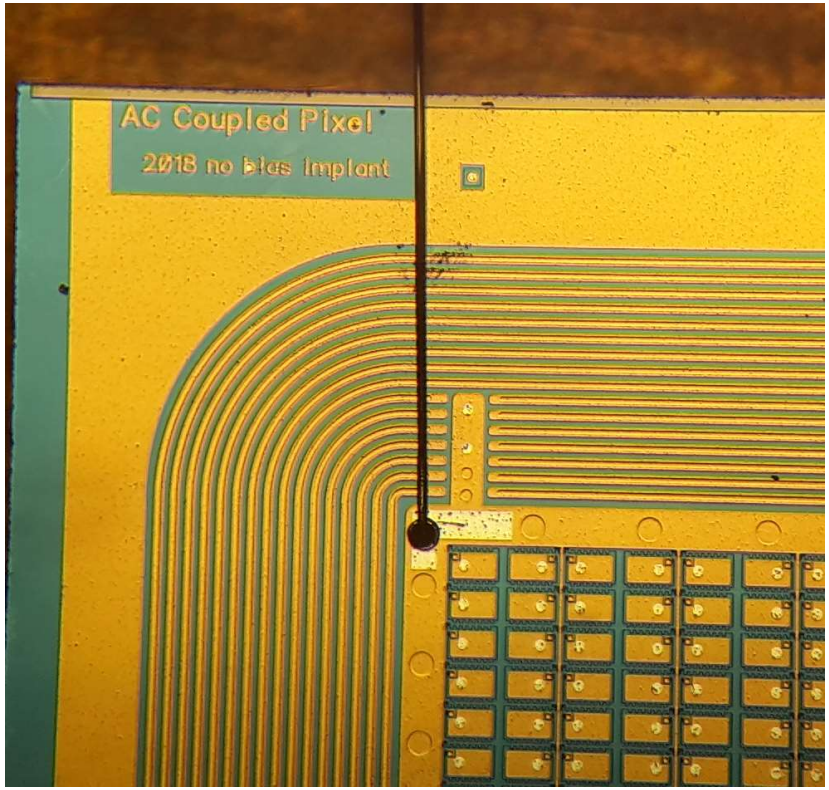




Spatially resolved Charge Collection Efficiency (CCE) of a pixel detector. The signal is excited by 2 MeV proton beam

Outline

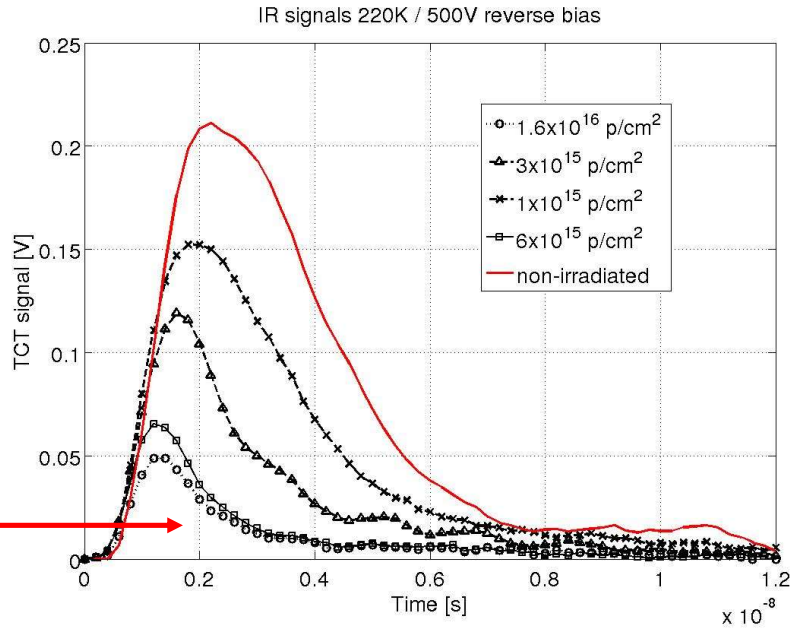
- Motivation and background
- Pixel detector design and layout
- Processing of detectors
- Characterization and selected results
- Summary and future prospectives

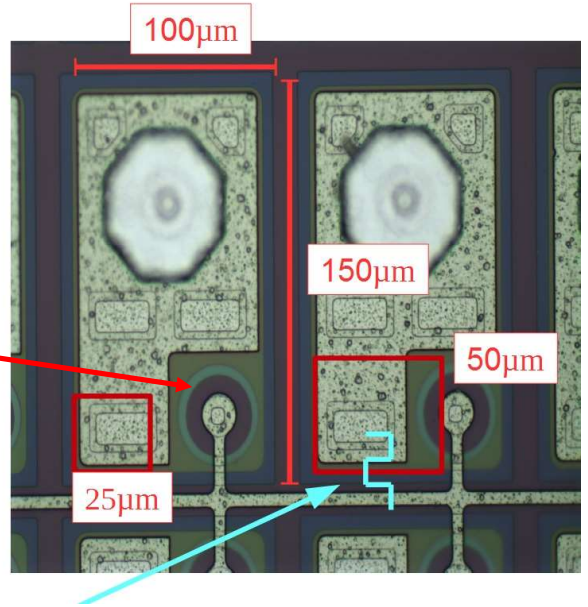


Motivation and background

Need for upgrades of existing detectors

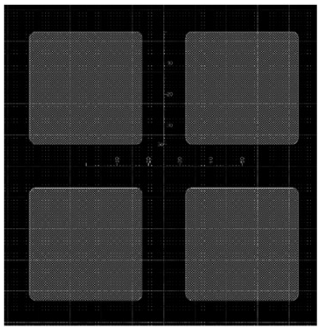
- Physicists want to discover more rare particle decay processes
- Luminosity of LHC must be increased to create more p->p collisions.
- More collisions means more radiation damage:
  - Signal degrades 100% -> 20% or less
  - Physical distance where electrons are collected degrades several hundreds of µm -> 20-40 µm.
- Pixels must be resistively connected with each other.
- Integrated bias resistors allow electrical quality assurance prior very expensive Flip-Chip bump bonding.



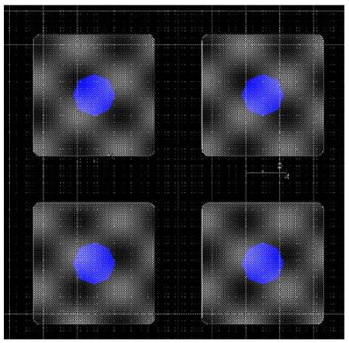


Detector design – RD53 pixel detector

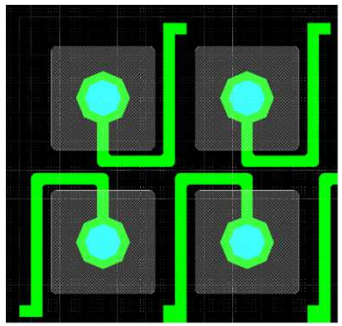
RD53 = CERN joint collaboration developing future CMOS read-out ASIC for all LHC experiments. Chip consist of 200 x 192 = 38400 pixels



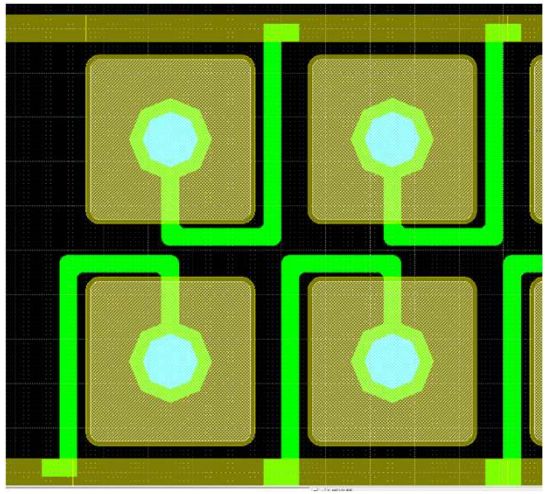
1st level – Implant



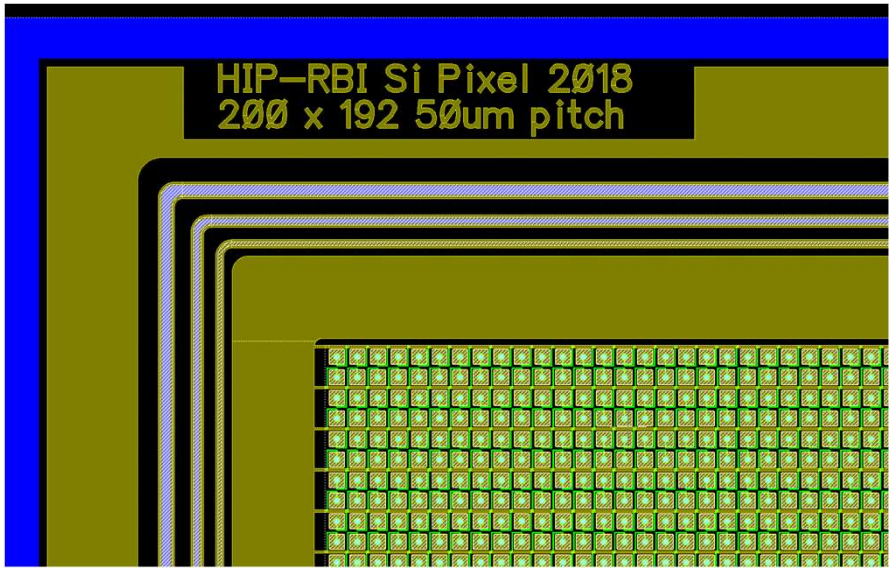
2nd level – contact opening to field insulator



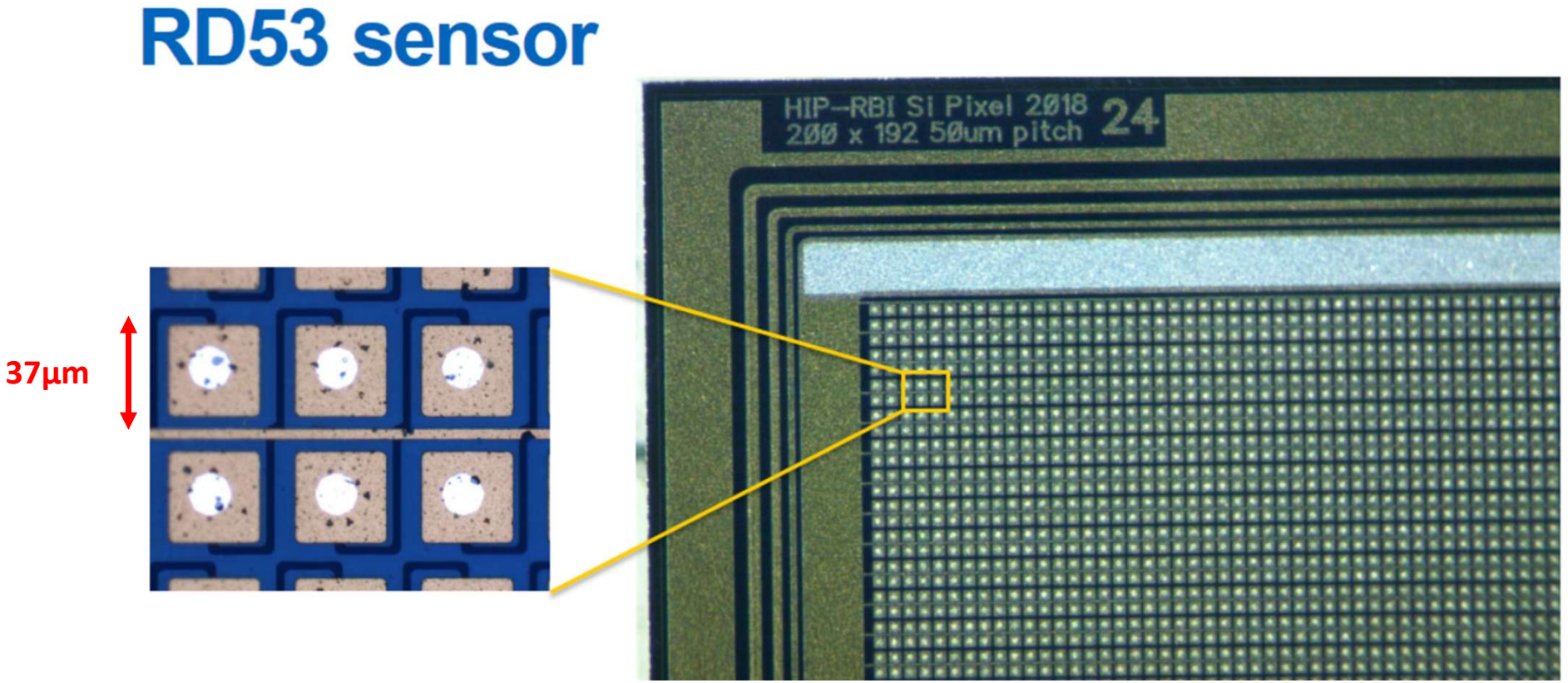
3rd level – bias resistor made of TiN deposited by Atomic Layer Deposition (ALD) method



4th level – metals



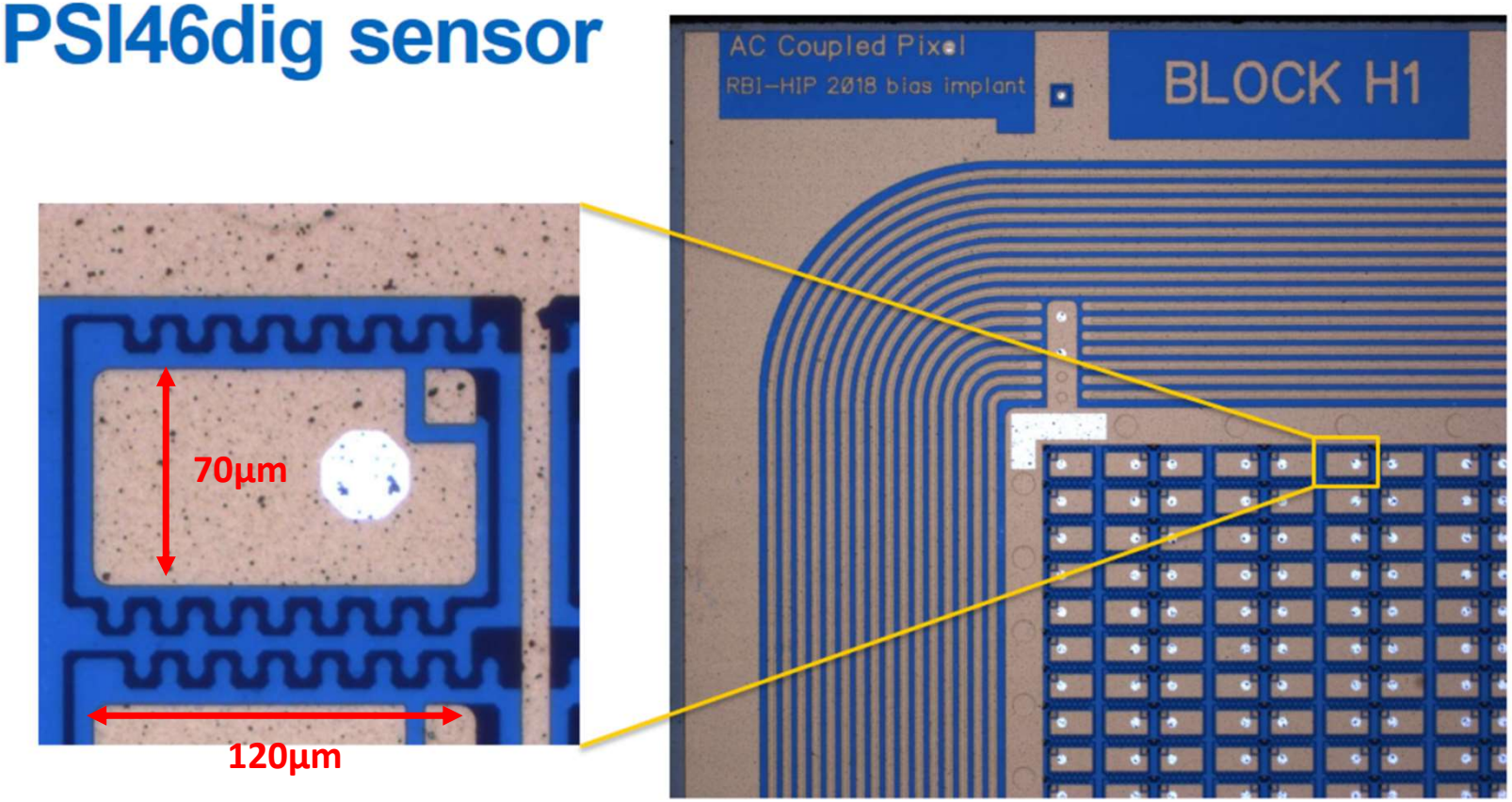
Detector design – RD53 pixel detector



Presented at 33rd RD50 Workshop, CERN, Geneva, Switzerland, November 28th 2018

J. Ott et al., ***Processing of pixel detectors on p-type MCz silicon using atomic layer deposition (ALD) grown aluminium oxide***
https://indico.cern.ch/event/754063/contributions/3222806/attachments/1760772/2865963/JOtt_RD50_Nov18_3.pdf

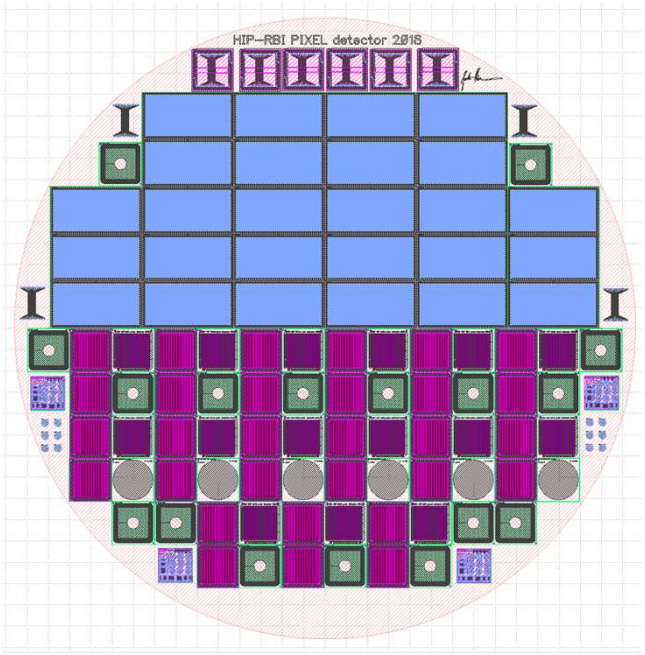
Detector design – PSI46dig pixel detector

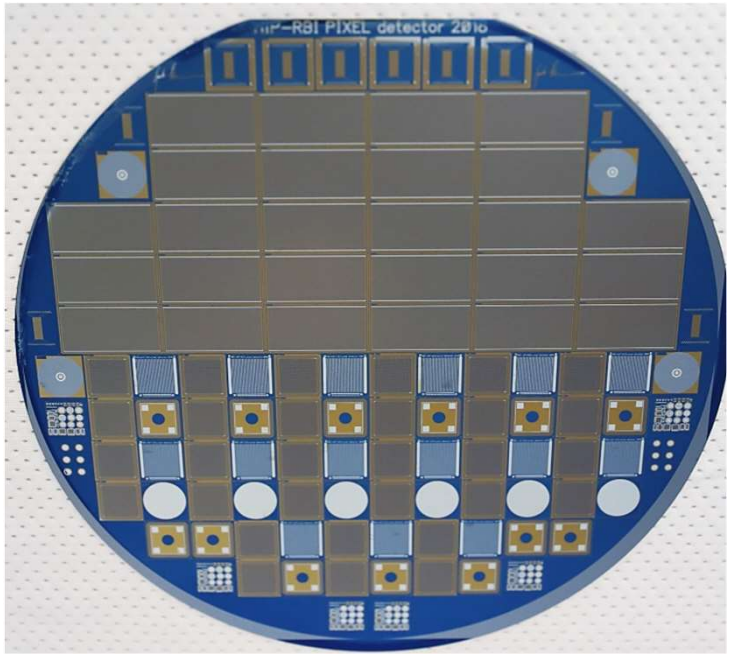


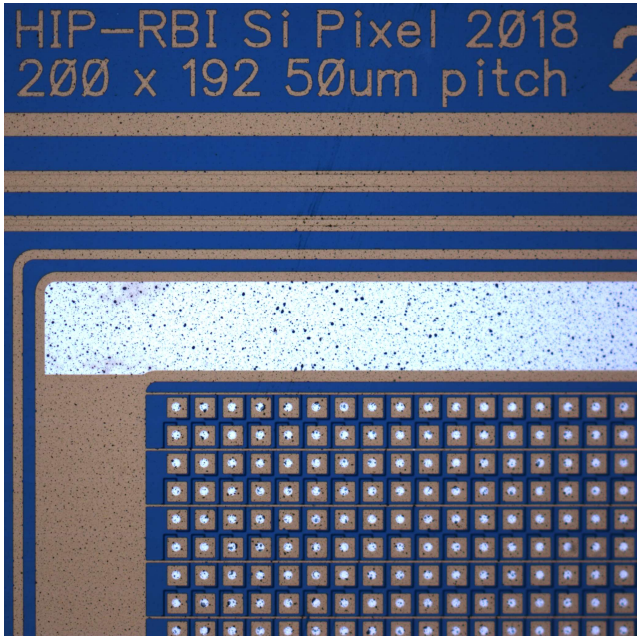
Presented at 33rd RD50 Workshop, CERN, Geneva, Switzerland, November 28th 2018

J. Ott et al., ***Processing of pixel detectors on p-type MCz silicon using atomic layer deposition (ALD) grown aluminium oxide***
https://indico.cern.ch/event/754063/contributions/3222806/attachments/1760772/2865963/JOtt_RD50_Nov18_3.pdf

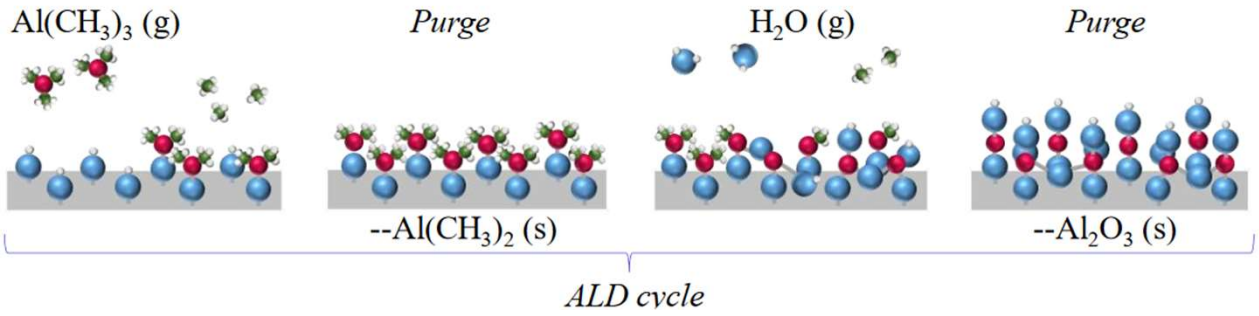
Processing of detectors

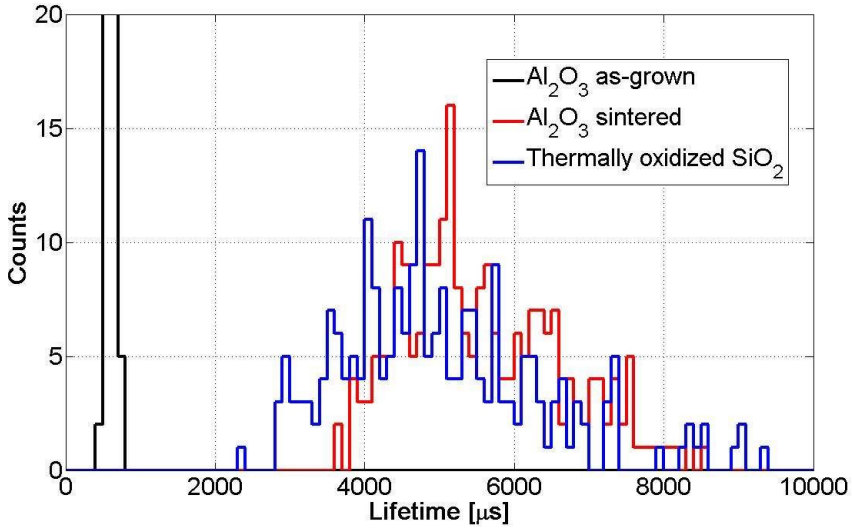


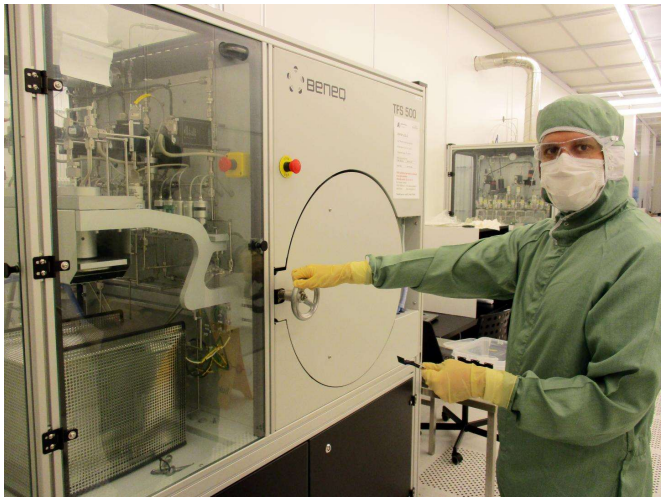




Passivation – Atomic Layer Deposition (ALD)



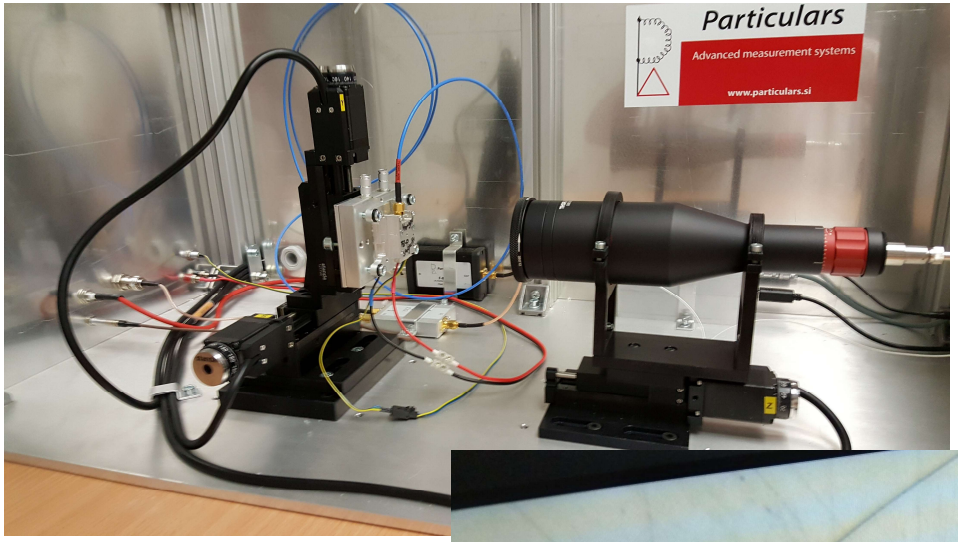


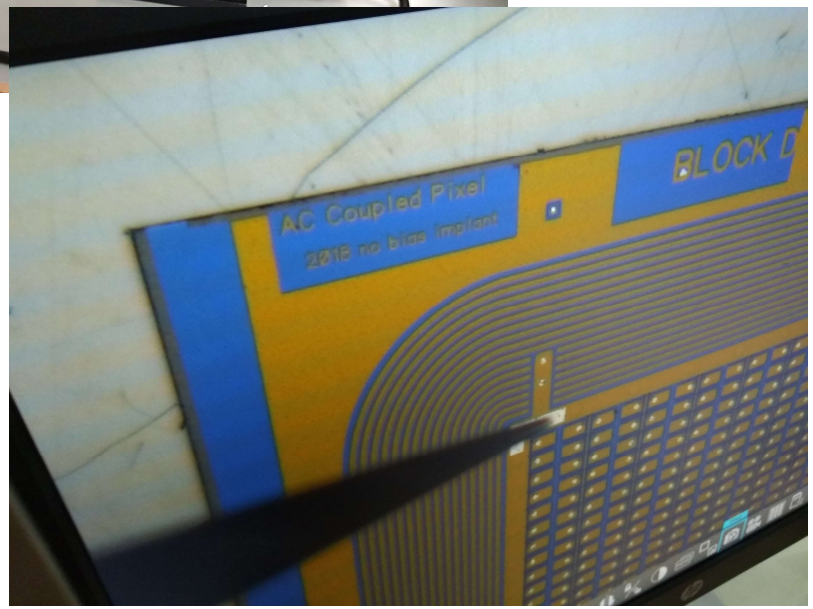


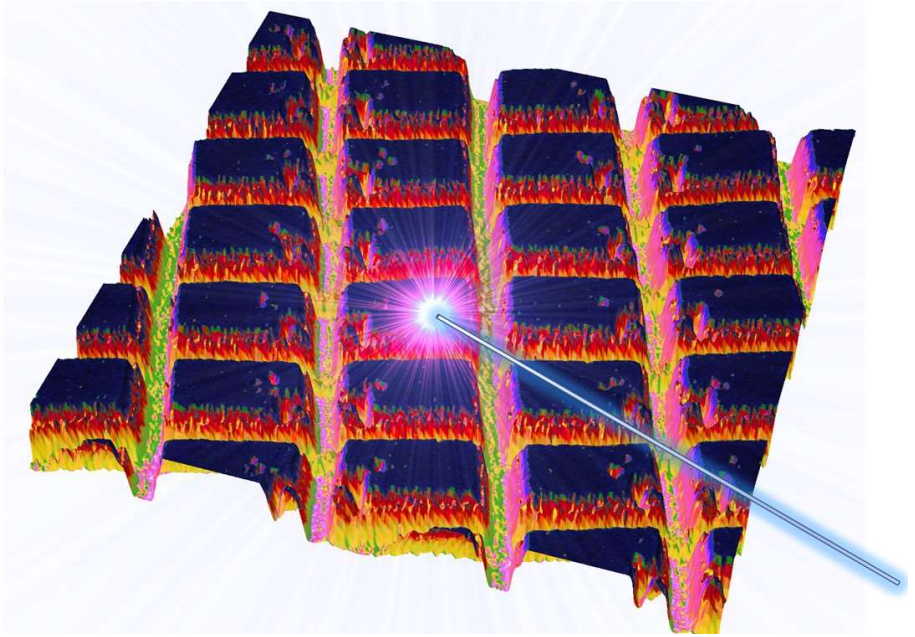
- The electrical passivation properties can be studied by lifetime (τ_{eff}) measurement
- τ_{eff} is combination of bulk lifetime (τ_{bulk}) and surface recombination (S_{srv}).
- High τ_{eff} can only be measured if S_{srv} → 0, i.e. Si surface is passivated.
- Thermally oxidized Si-SiO_2 interface is known to produce best possible S_{srv} → 0
- Oxidized p-type reveals bulk lifetime (τ_{bulk}) (BLUE distribution) and thus it is reference value for passivation studies.
- SiO_2 is removed → ALD Al_2O_3 deposition + repeated lifetime measurement (RED distribution).
- Good passivation (S_{srv} → 0) is achieved by field effect, **negative oxide oxide charge in Al_2O_3** is repulsing e- to recombinate into surface states.

- J. Härkönen et al., "Processing of n+/p−/p+ strip detectors with atomic layer deposition (ALD) grown Al2O3 field insulator on magnetic Czochralski silicon (MCz-si) substrates", NIMA 826, 2016
- J. Härkönen et al., Atomic Layer Deposition (ALD) grown thin films for ultra-fine pitch pixel detectors, NIMA 831, 2016
- J. Ott et al., *Processing of AC-coupled n-in-p pixel detectors on MCz silicon using atomic layer deposited aluminium oxide*, in VCI 2019 - The 15th Vienna Conference on Instrumentation, February 20, 2019

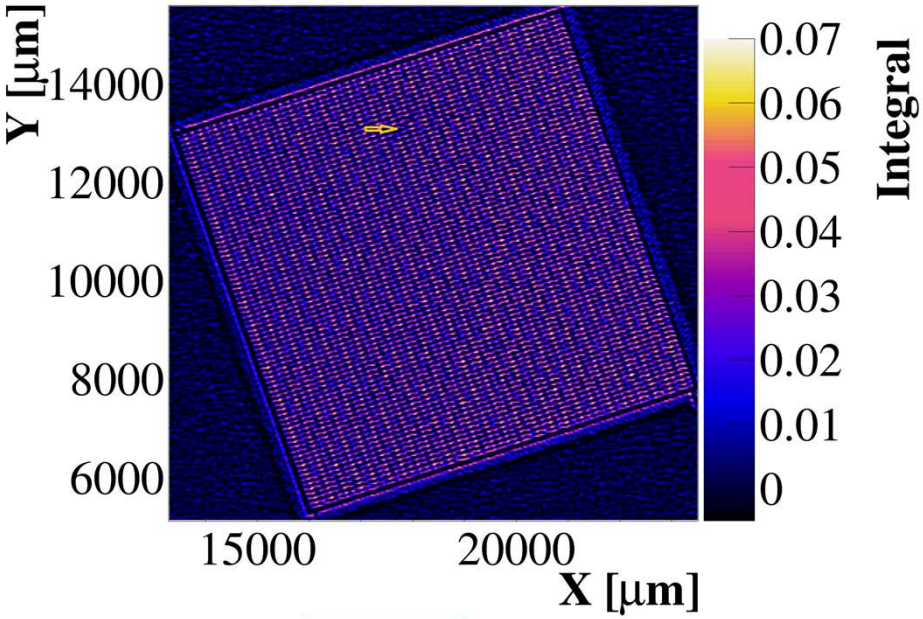
Characterization and selected results



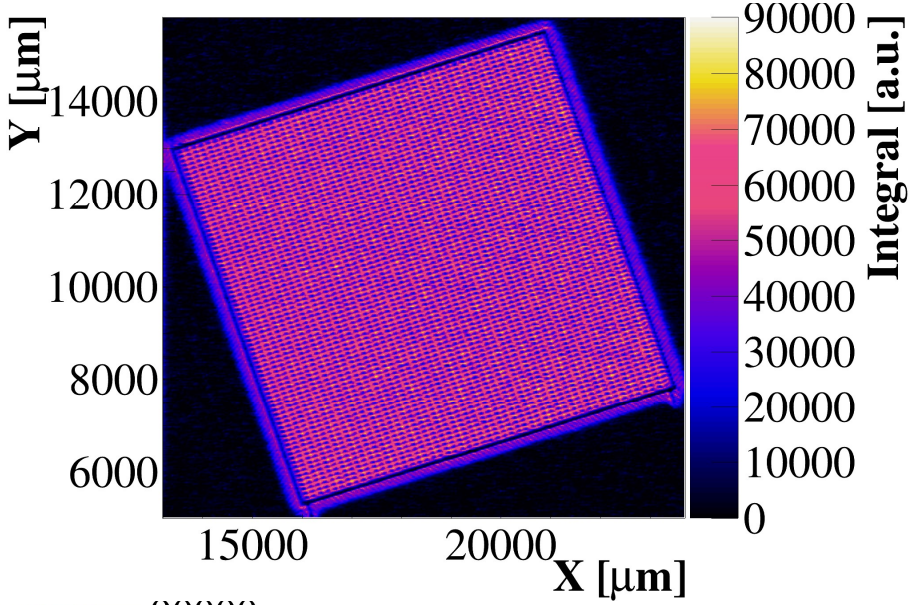




TCT xy-area scans for pixel detectors

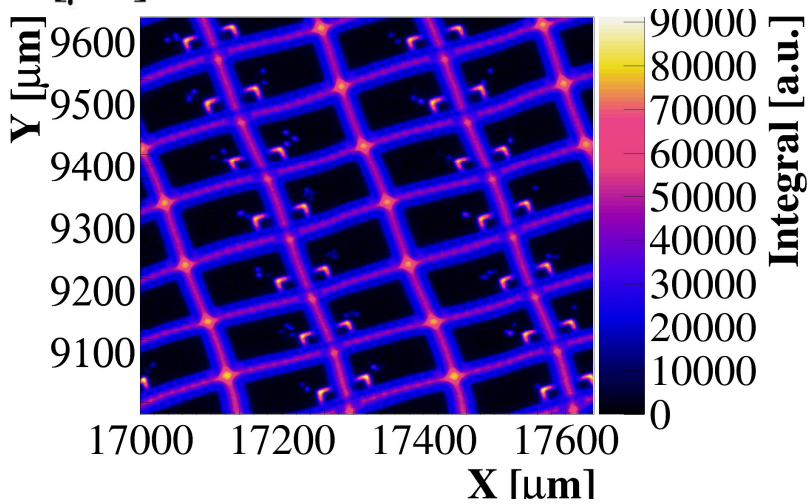


670nm

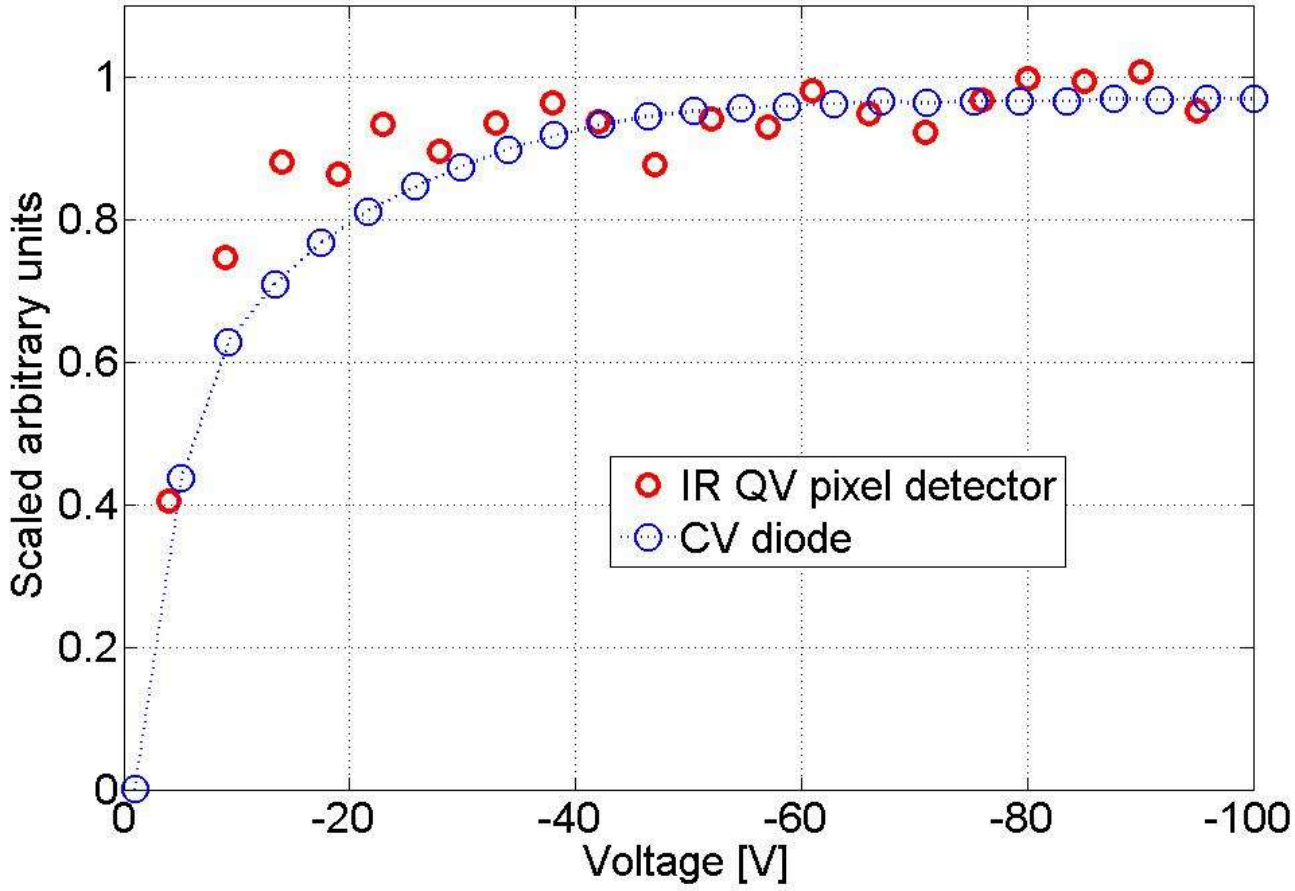


1160nm

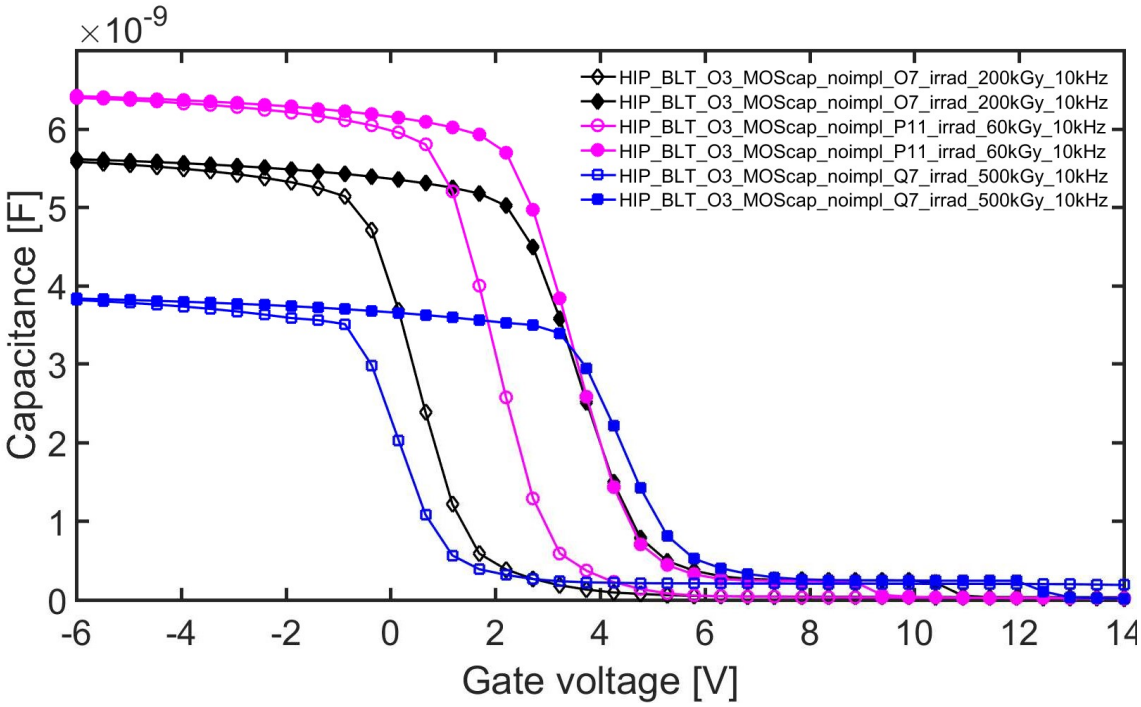
- Each TCT xy-scan is about 60 000 data points.
- The amplitude of the signal is converted into color scale.

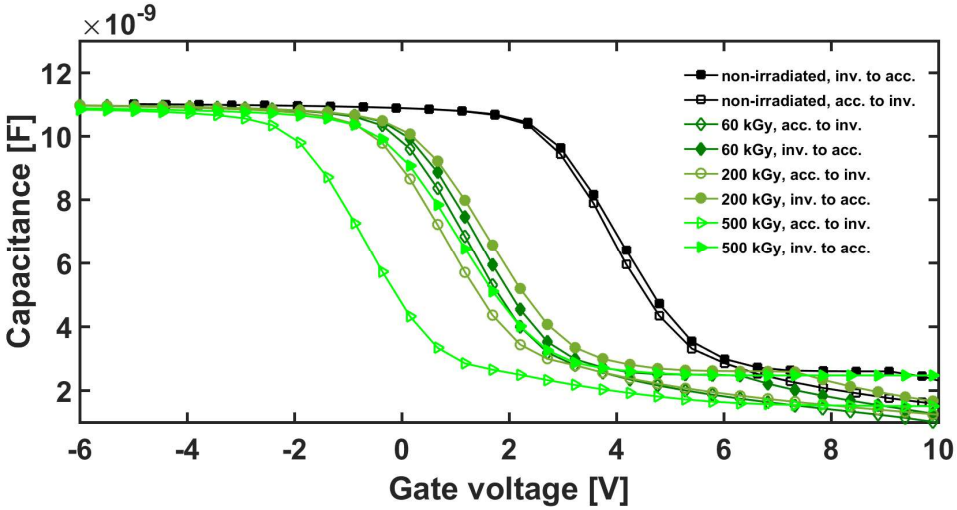


Full depletion voltage V_{fd}



^{60}Co gamma irradiation – MOS V_{fb}

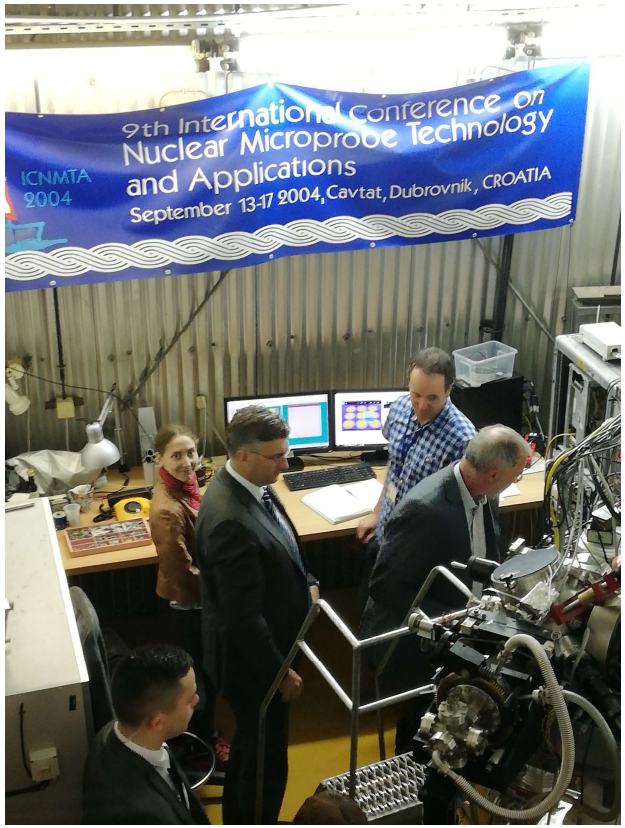




Summary

- Helsinki Institute of Physics (HIP) and RBI PaRaDeSeC teams have on-going common activity to develop new and innovative pixel detectors intented for CMS Phase II Upgrade.
- We have simulated, designed, manufactured and characterized novel fine pitch $n^+/p^-/p^+$ pixel detectors made on 150mm size p-type Magnetic Czochralski silicon (p-MCz Si) wafers.
- Detectors are processed at Micronova nanofabrication center in Finland (www.micronova.fi)
- Atomic Layer Deposition (ALD) technology has many properties, which make it very attractive process method for radiation detectors.
- With ALD technology it is possible to realize very high capacitance and resistance densities.
- This enables AC-coupling of small pixels connected with each other by metal-nitride thin film bias resistors.
- Our (yet unpublished) results show that during the ^{60}Co gamma irradiation the ’fixed oxide charge” remains rather unchanged but positive “mobile ionic oxide charge” accumulates.
- After neutron –irradiation negative net oxide increases.
- Flip-Chip bonding of experimental pixel sensors with CMS ROC chips foreseen in the near future.

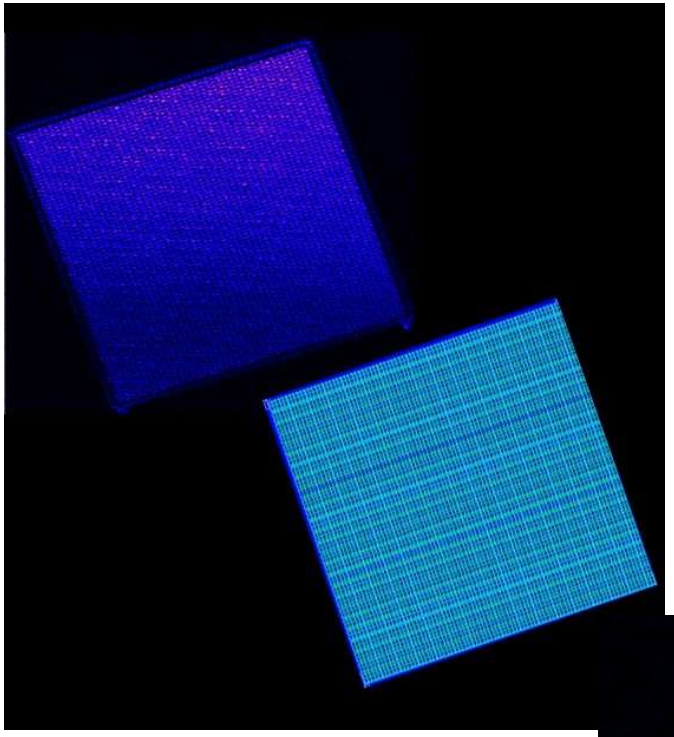
HELSINKI INSTITUTE OF PHYSICS

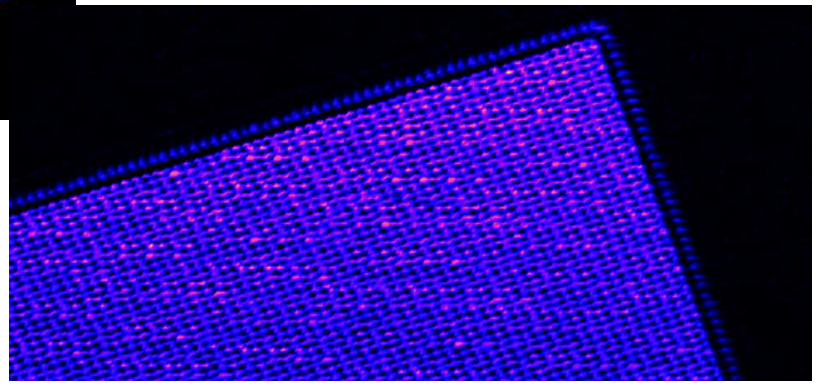


Jenni Ott (HIP) and Matti Kalliokoski (RBI) measuring pixel detector at the Ruđer Bošković Institute Focused Ion Beam facility.

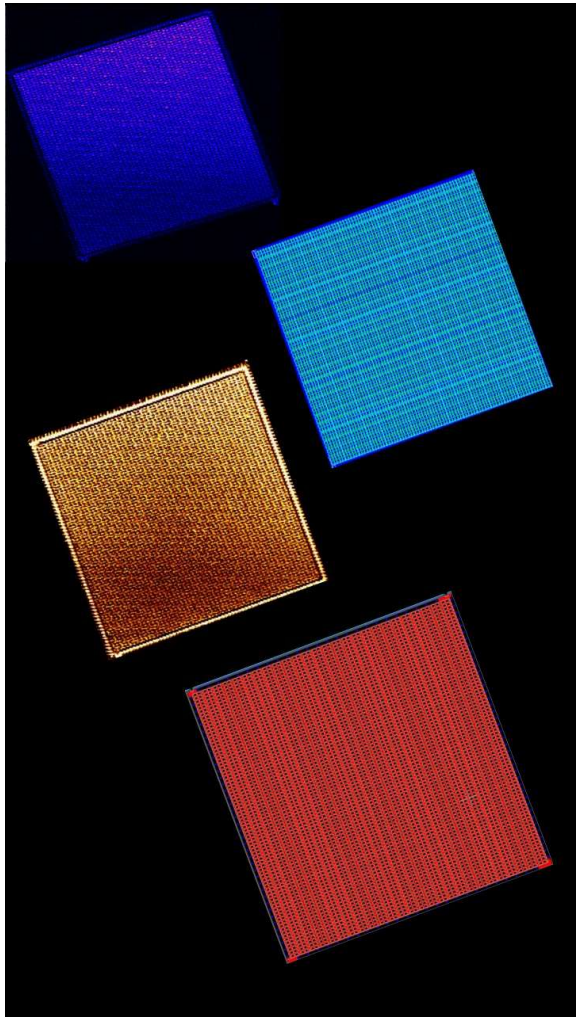
Backup slides

When pixel technology meets Arts....





Each square is TCT xy-scan of about 60 000 data points.
The amplitude of the signal is converted into color scale.



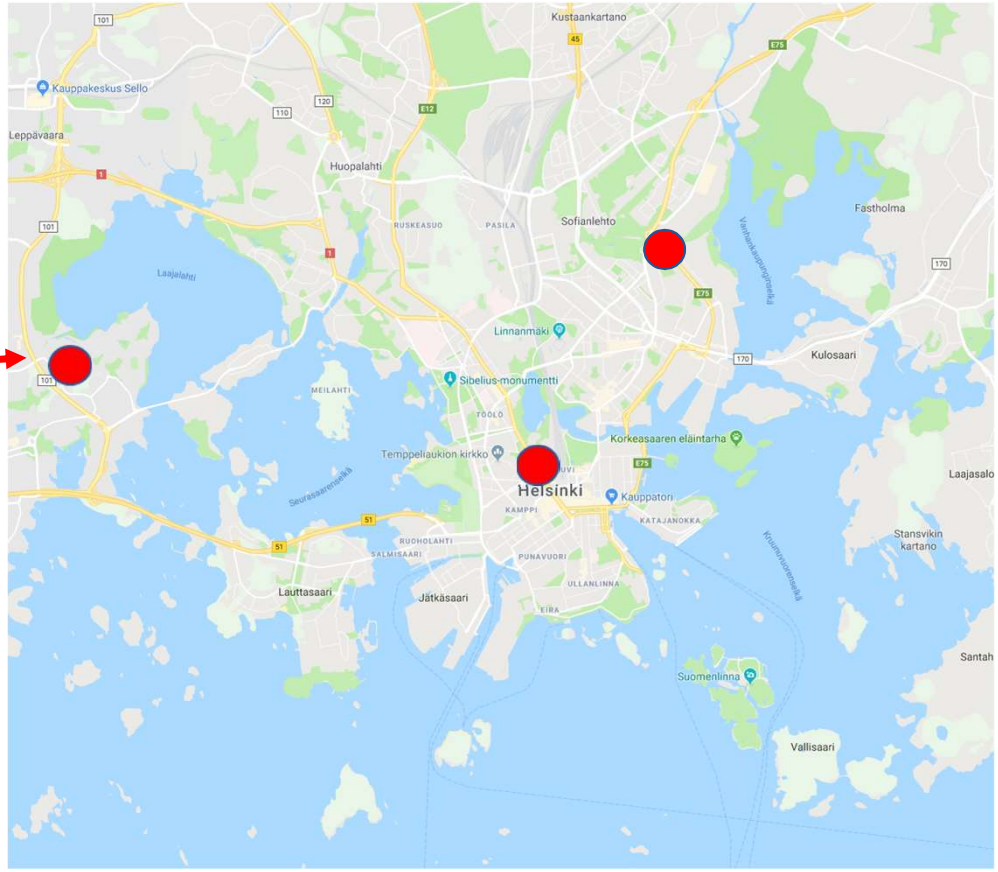
Backup slides

When pixel technology meets Arts....

Eija Tuominen's cat "Tessa" in front of pixel Arts

Backup slides

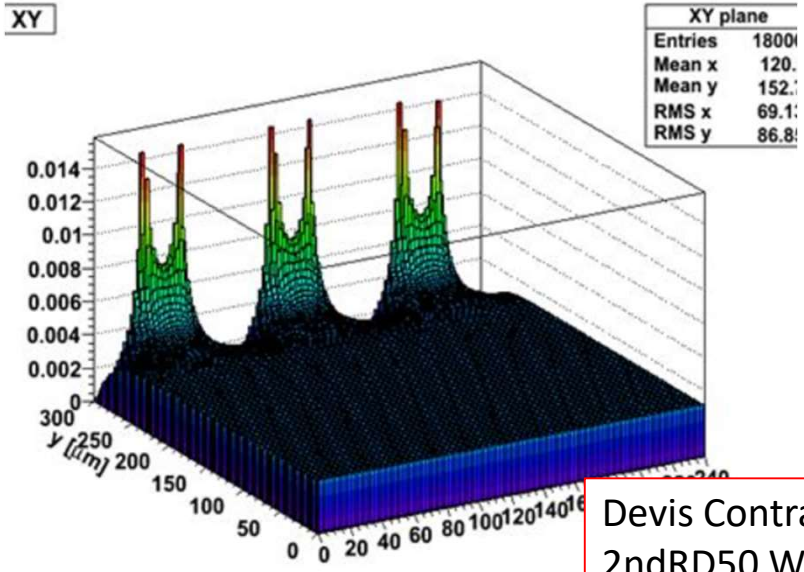
-Micronova facility

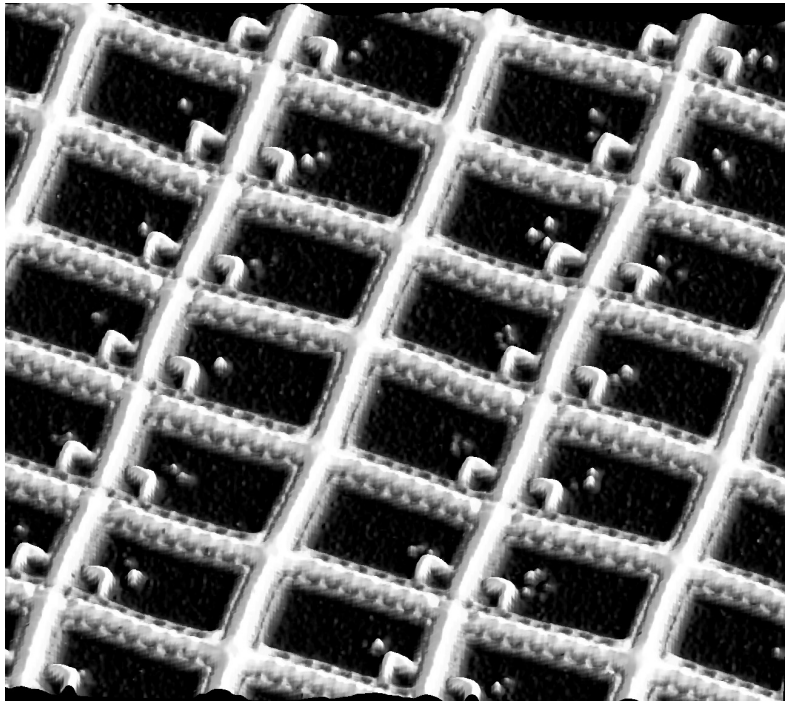


Backup slides

- Patterning a thin entrance window to side of the illumination

- The back side, i.e. side of illumination of a pixel detector can can be patterned mesh-like by one additional mask level.
- The metal grid can be formed e.g. by TiW/W/Al layers
- Metal grid forms a hard mask for RIE etching
- p^+ implant on windows is removed by plasma etching
- Entrance window is finished by thin ~2-4nm ALD dielectric layer
- Pixelated back side is assumed to form Weighting Field and thus to enhance CCE





Laser scan of pixelated back side

Devis Contrato and Gregor Kramber
2ndRD50 Workshop - CERN, 18-20 May 2003